Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 - 82 (CANCELLED).

83. (NEW) A method for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode using a global scan enable (global_SE) signal and one or more global set/reset enable (global_SR_EN) signals, the scan-based integrated circuit containing one or more set/reset circuitries each controlled by a set/reset controller, and one or more scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller connected to said global scan enable (global_SE) signal and one said global set/reset enable (global_SR_EN) signal; said method comprising:

(a) shifting in a stimulus to all said scan cells in said scan-based integrated circuit by enabling said global scan enable (global_SE) signal through all said set/reset controllers to disable all said set/reset circuitries during a shift-in operation;

(b) capturing a test response of all said scan cells for testing said faults propagated to said data ports and said

20   asynchronous set/reset ports of all said selected scan cells by enabling or disabling selected global set/reset enable (global_SR_EN) signals while disabling said global scan enable (global_SE) signal during a capture operation;

(c)   shifting out said test response for comparison or compaction

25   while shifting in a new stimulus to all said scan cells during a shift-out operation.

84.   (NEW)   The method of claim 83, wherein said shifting in a stimulus to all said scan cells further comprises selectively shifting in a predetermined stimulus from an ATE (automatic test equipment) in said selected scan-test mode or shifting in a pseudo-

5   random stimulus automatically generated in said scan-based integrated circuit using a pseudo-random pattern generator (PRPG) in said selected self-test mode during said shift-in operation.

85.   (NEW)   The method of claim 83, wherein said global scan enable (global_SE) signal is further used to enable shifting a scan data from a first scan cell to a second scan cell during said shift-in and said shift-out operation.

86.   (NEW)   The method of claim 83, wherein said capturing a test response of all said scan cells further comprises disabling all said clocks controlling all said scan cells, while enabling all said selected global set/reset enable (global_SR_EN) signals, for

5   testing said faults propagated to said asynchronous set/reset ports

of said selected scan cells during said capture operation.

87. (NEW)   The method of claim 86, wherein said enabling all

said selected global set/reset enable (global_SR_EN) signals

further comprises selectively enabling two or more said selected

global set/reset enable (global_SR_EN) signals simultaneously or in

5   an ordered sequence during said capture operation.

88. (NEW)   The method of claim 83, wherein said capturing a

test response of all said scan cells further comprises enabling all

said clocks controlling all said scan cells, while disabling all

said selected global set/reset enable (global_SR_EN) signals, for

5   testing said faults propagated to said data ports of all said

selected scan cells during said capture operation.

89. (NEW)   The method of claim 88, wherein said enabling all

said clocks controlling all said scan cells further comprises

selectively enabling two or more said clocks controlling two or

more said scan cells simultaneously or in an ordered sequence

5   during said capture operation.

90. (NEW)   The method of claim 83, wherein said shifting out

said test response for comparison or compaction further comprises

selectively shifting out said test response to said ATE for

comparison in said selected scan-test mode or shifting out said

5   test response for compaction using a compactor, including a

multiple-input signature register (MISR), in said selected self-

test mode during said shift-out operation.

91. (NEW)   The method of claim 83, wherein said set/reset

controller further comprises providing a shift controller and a

capture controller in response to said global scan enable

(global_SE) signal and a said global set/reset enable

5   (global_SR_EN) signal, wherein said shift controller is adapted to

disable said asynchronous set/reset ports of one or more said

selected scan cells during said shift-in or said shift-out

operation, and wherein said capture controller is adapted to enable

or disable propagation of said faults present in one said set/reset

10   circuitry to said asynchronous set/reset ports of one or more said

selected scan cells during said capture operation.

92. (NEW)   The method of claim 83, wherein said global scan

enable (global_SE) signal is selectively generated in said scan-

based integrated circuit or an input signal to said scan-based

integrated circuit.

93. (NEW)   The method of claim 83, wherein said global

set/reset enable (global_SR_EN) signal is selectively generated in

said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

94. (NEW)   The method of claim 83, wherein said scan cell is selectively a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

95. (NEW)   The method of claim 83, wherein said set/reset controller is used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset

5   violations, and destructive set/reset violations, in a selected set/reset circuitry in said scan-based integrated circuit.

96. (NEW)   A set/reset controller having a global scan enable (global_SE) signal and a global set/reset enable (global_SR_EN) signal for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based

5   integrated circuit, the scan-based integrated circuit containing one or more set/reset circuitries and one or more scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks; said set/reset controller comprising:

10   (a)   a shift controller, inserted between a selected set/reset circuitry and said asynchronous set/reset ports of all said

selected scan cells, for disabling said asynchronous set/reset ports of all said selected scan cells, when said global scan enable (global_SE) signal is enabled, during a shift-in or a

15 shift-out operation; and

(b) a capture controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for enabling or disabling propagation of said faults present in said selected set/reset circuitry to

20 said asynchronous set/reset ports of all said selected scan cells, in response to said global set/reset enable (global_SR_EN) signal when said global scan enable (global_SE) signal is disabled, during a capture operation.

97. (NEW) The set/reset controller of claim 96, wherein said shift controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells, and wherein said global scan enable (global_SE) signal, said global set/reset enable

5 (global_SR_EN) signal, or said global scan enable (global_SE) signal and said global set/reset enable (global_SR_EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

98. (NEW) The set/reset controller of claim 96, wherein said global scan enable (global_SE) signal is further used to enable

shifting a scan data from a first scan cell to a second scan cell during said shift-in and said shift-out operation.

99. (NEW)   The set/reset controller of claim 96, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling said global set/reset enable (global_SR_EN) signal, for testing said faults

5   propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

100. (NEW)   The set/reset controller of claim 96, wherein said capture controller further comprises enabling all said clocks controlling all said scan cells, while disabling said global set/reset enable (global_SR_EN) signal, for testing said faults

5   propagated to said data ports of said selected scan cells during said capture operation.

101. (NEW)   The set/reset controller of claim 100, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered

5   sequence during said capture operation.

102. (NEW)   The set/reset controller of claim 96, wherein said capture controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells.

103. (NEW)   The set/reset controller of claim 96, wherein said global scan enable (global_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

104. (NEW)   The set/reset controller of claim 96, wherein said global set/reset enable (global_SR_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

105. (NEW)   The set/reset controller of claim 96, wherein said scan cell is selectively a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

106. (NEW)   The set/reset controller of claim 96, wherein said shift controller and capture controller are used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinationally-gated set/reset violations, generated set/reset violations, and destructive

set/reset violations, in said selected set/reset circuitry in said scan-based integrated circuit.